S/N 09/256,643 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al. Examiner: Michael Trinh
Serial No.: 09/256,643 Group Art Unit: 2822
Filed: February 23, 1999 Docket: 303.324US2
Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

RESPONSE TO RESTRICTION REQUIREMENT AND PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Prior to examination, please amend the above-identified application as follows:

ELECTION/RESTRICTION

In response to the Restriction Requirement mailed March 14, 2000, Applicants elect, without traverse, Group I (claims 21-33). Applicants respectfully cancel remaining claims 34-35 without prejudice, and reserve the right to reintroduce them in a divisional application at a later date.

IN THE CLAIMS

Please amend the following claims:

21.(Amended) A method of [producing] fabricating a transistor [on] in a semiconductor substrate, the method comprising:

forming a source region and a drain [regions] region in a semiconductor substrate, [thereby defining] a channel region being between the source region and the drain region [regions];

forming an insulating layer on the channel region; and

forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$; and

selecting x at a predetermined value approximately between 0 and 1.0.

29.(Amended) The method of claim 21, wherein [fabricating the gate includes the steps of] forming a gate further comprises:

depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer using low pressure